G-2 Tracker Electronics Update

Detailed documentation:
http://edf.bu.edu/G-2

Newest Group Member

Dan Gastler

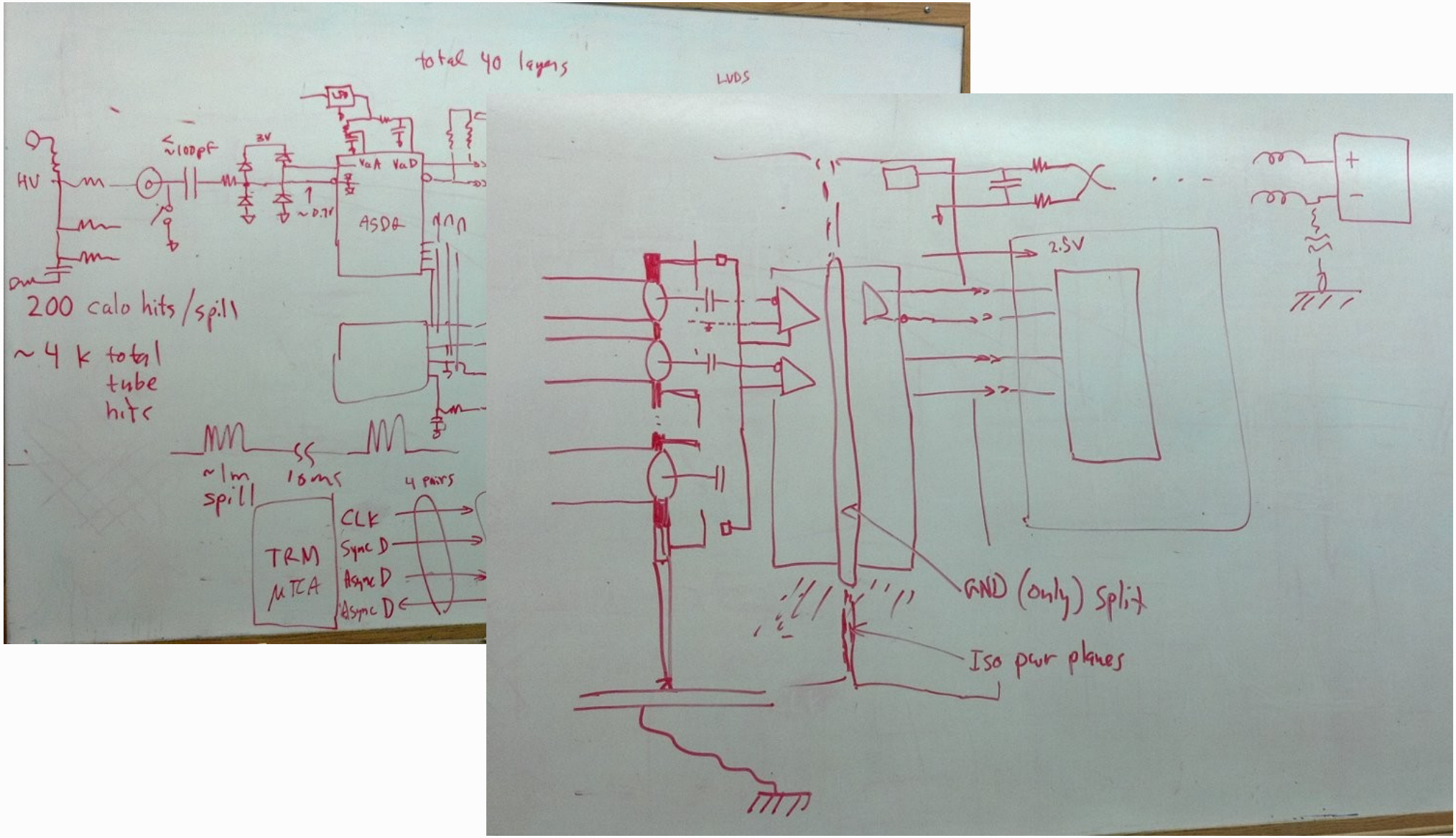
- BU Ph.D. 2012 (Physics)
- BSEE in Physics & Applied Math from U-MN Duluth
- Designed and implemented DAQ for MiniCLEAN and MicroCLEAN
- Significant PCB design and FPGA programming experience

He is now a full-time member of the EDF staff, and will initially be responsible for the commissioning of the on-chamber tracker electronics

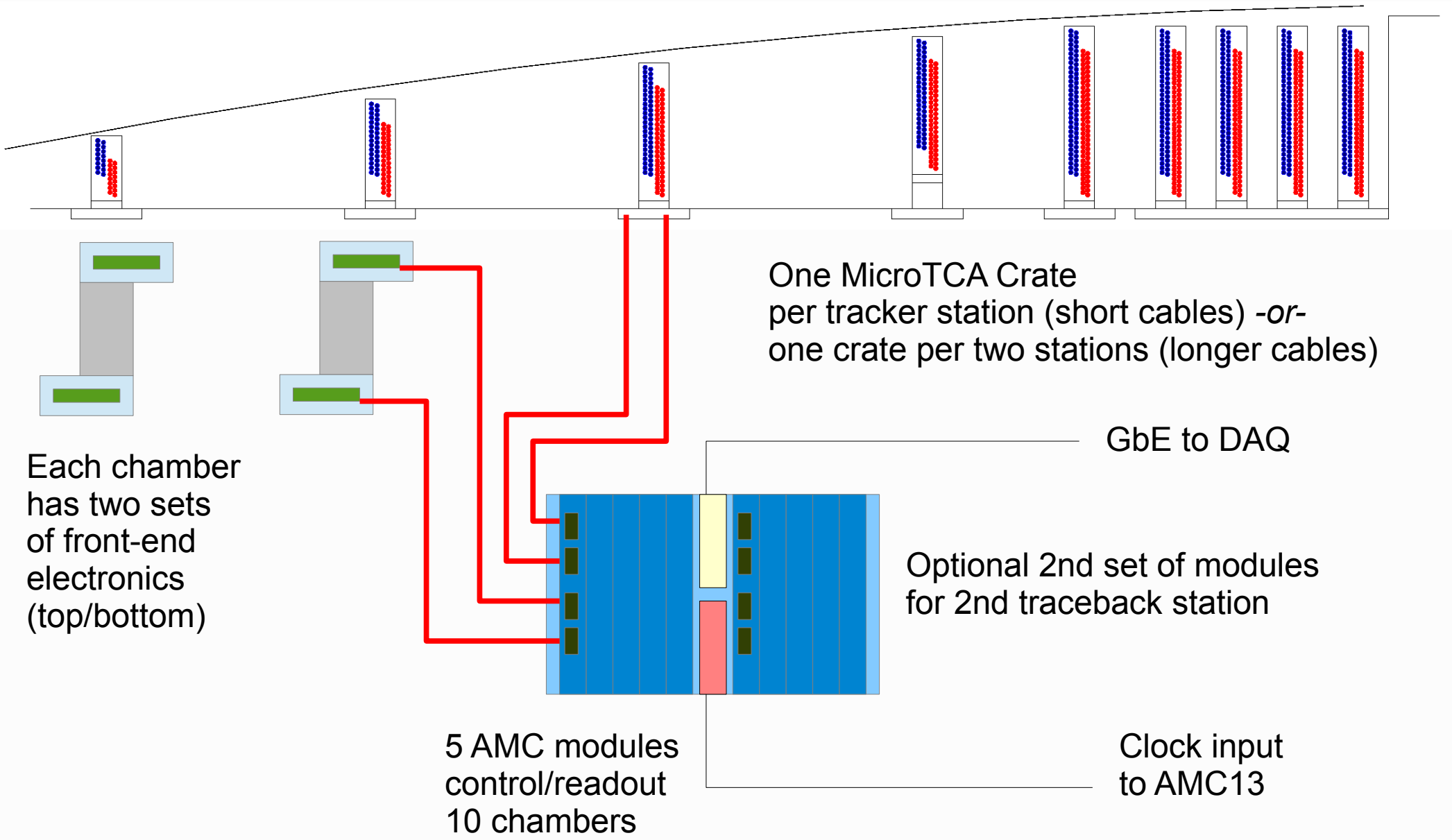
Introduction

- On-chamber electronics
  - ASDQ and TDC boards back from Assembly
  - Testing just starting
- Test Fixture (“flight simulator”)
  - PCBs back being assembled
- Readout Module (TRM)
  - “Phase I” firmware completed
- Firmware / DAQ software collaboration
  - Discussions underway with UK colleagues

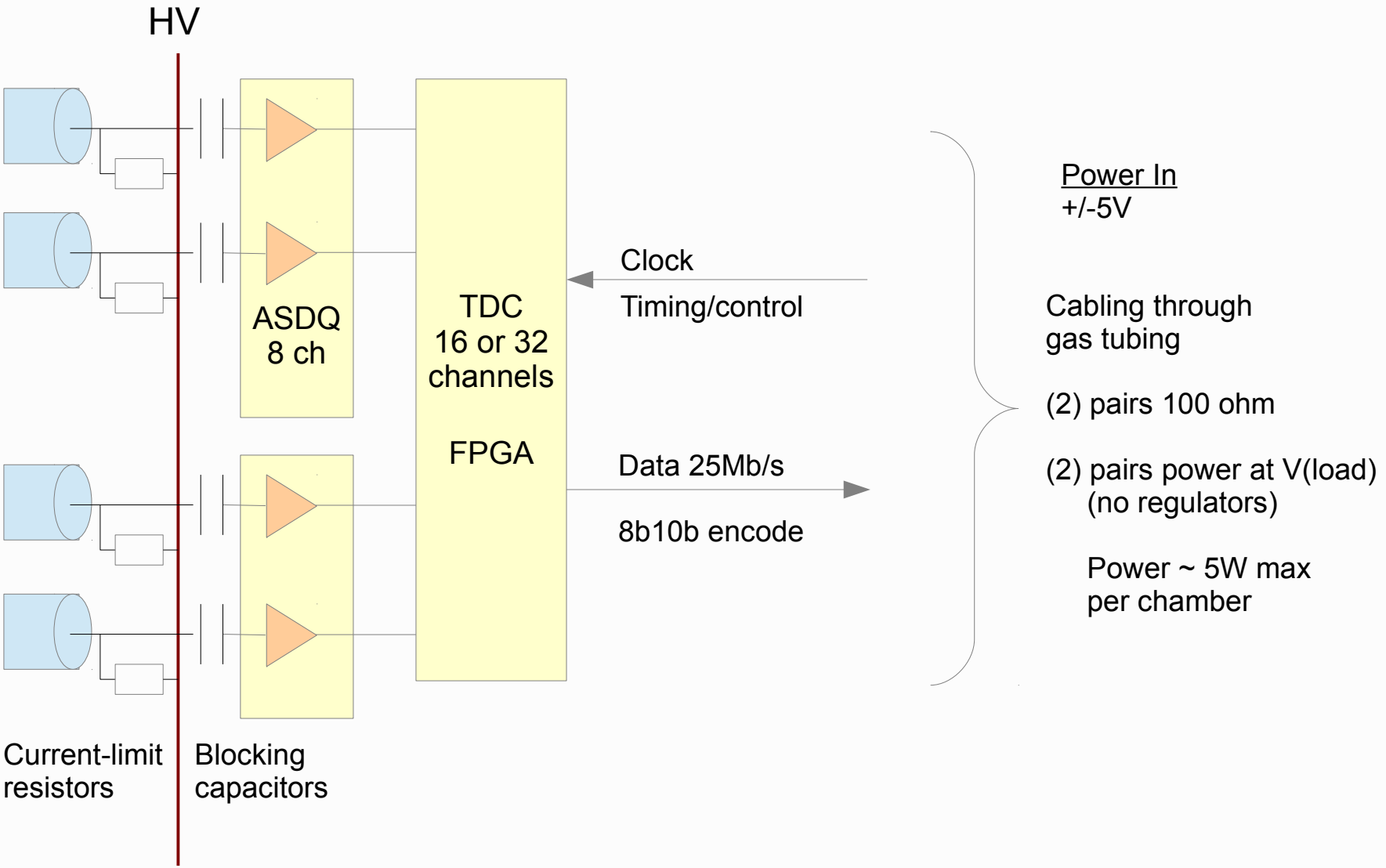
January 2013...



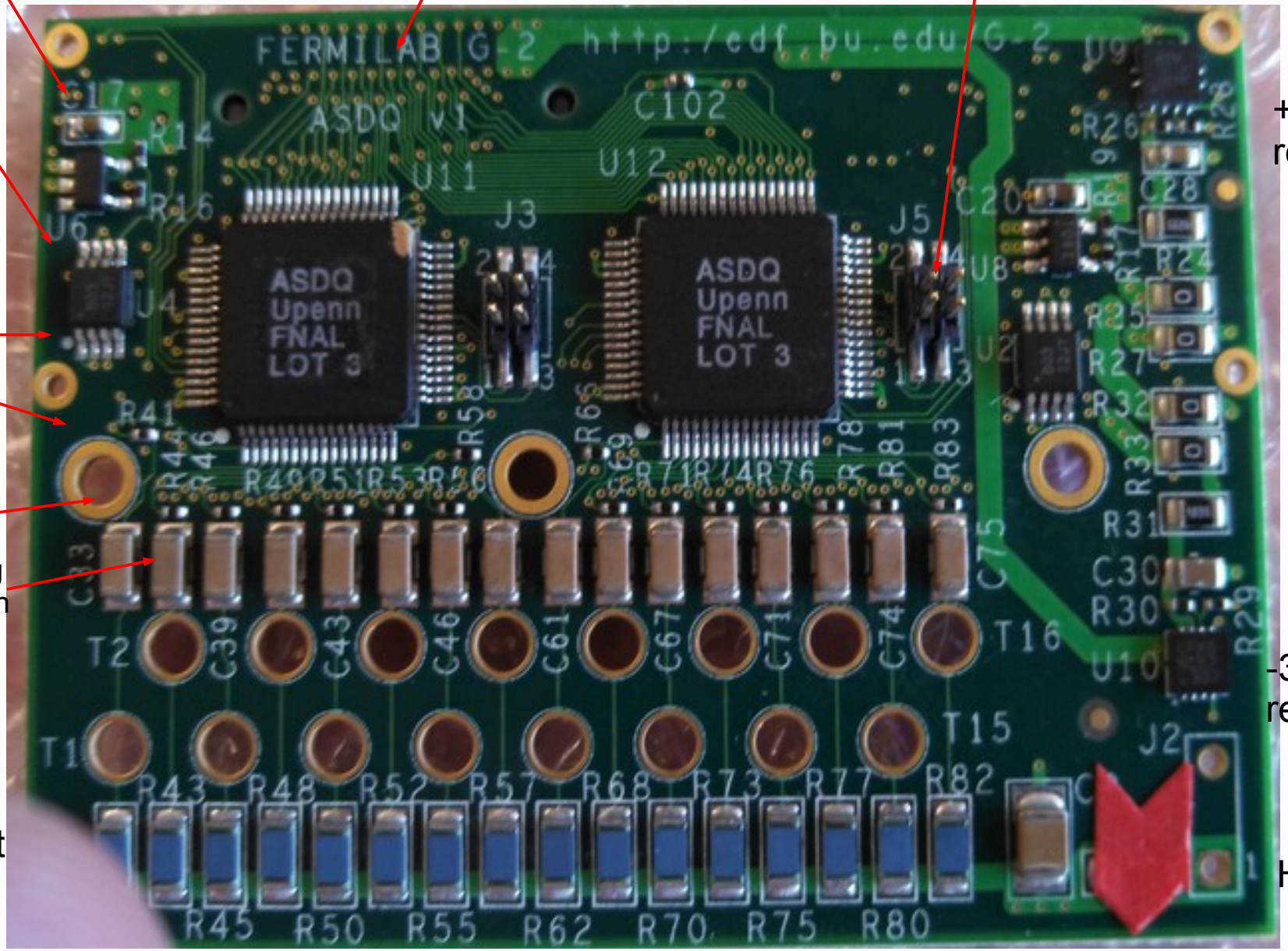
Tracker Electronics Overview



On-Chamber Electronics Overview
(prototype 16 channel module)



Now! - ASDQ Board



V+1.6

V+3D

V+3A

V-3A

GND standoffs

HV decoupling ESD protection

Straw inputs

HV current limit Rs

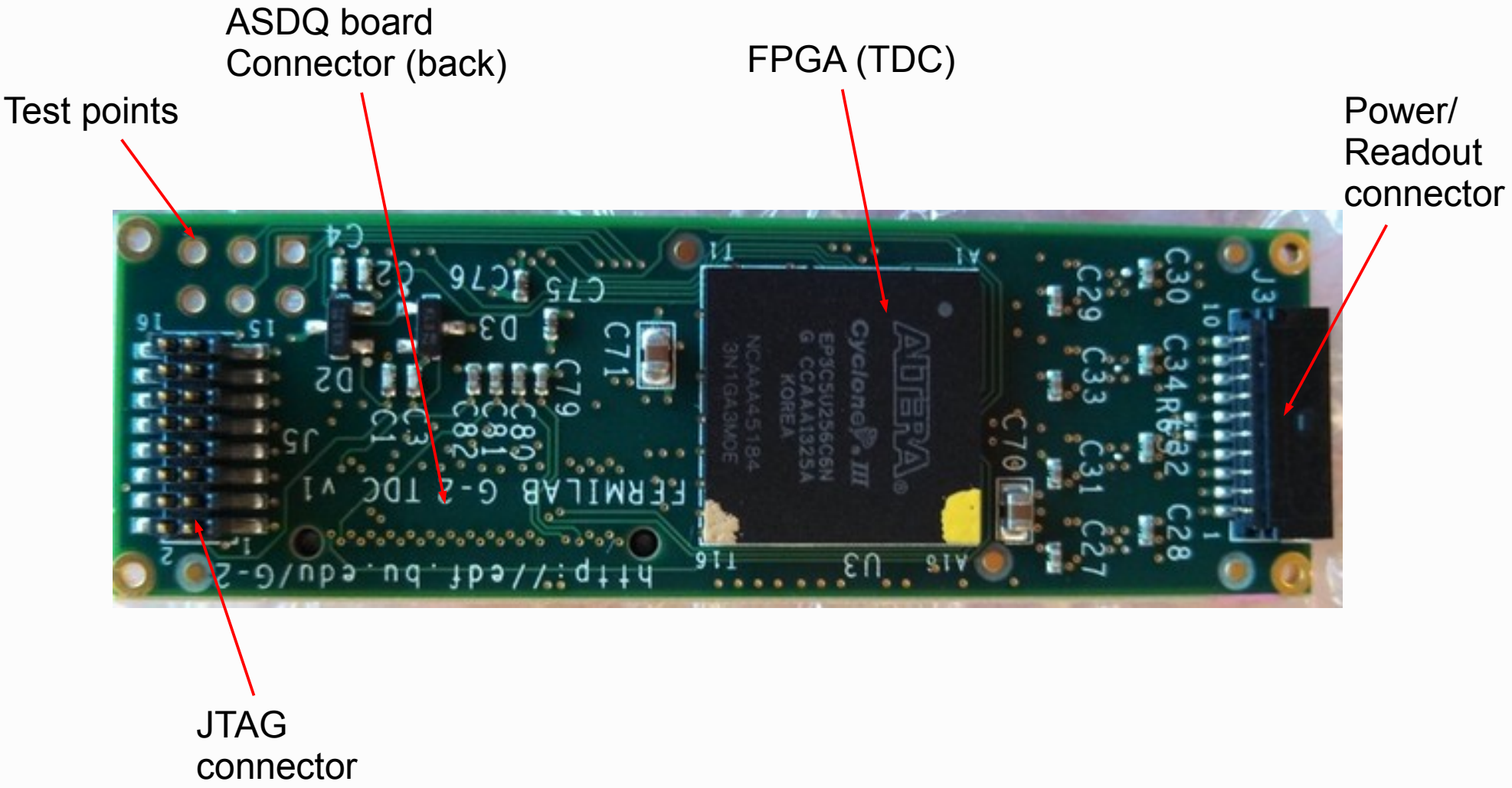
Analog output test connectors

+3V regulator

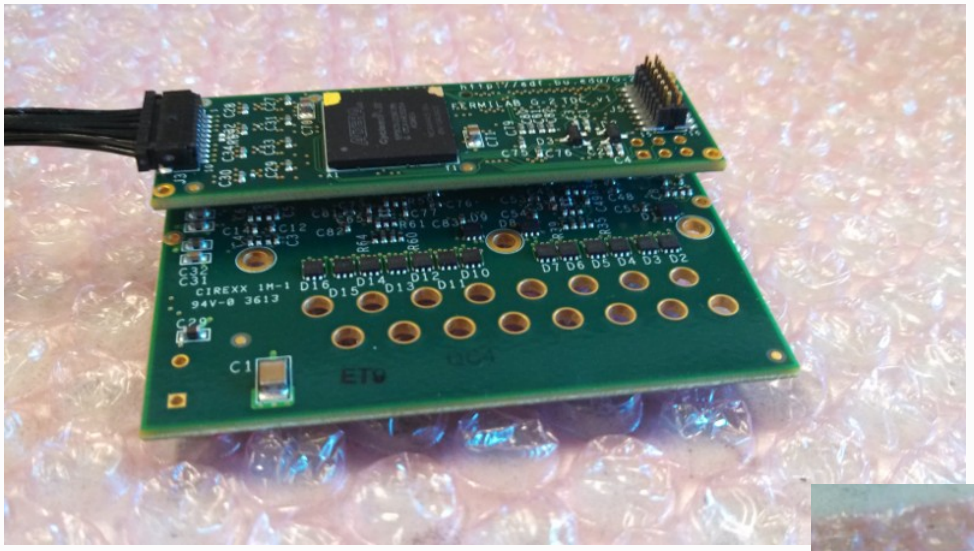
-3V regulator

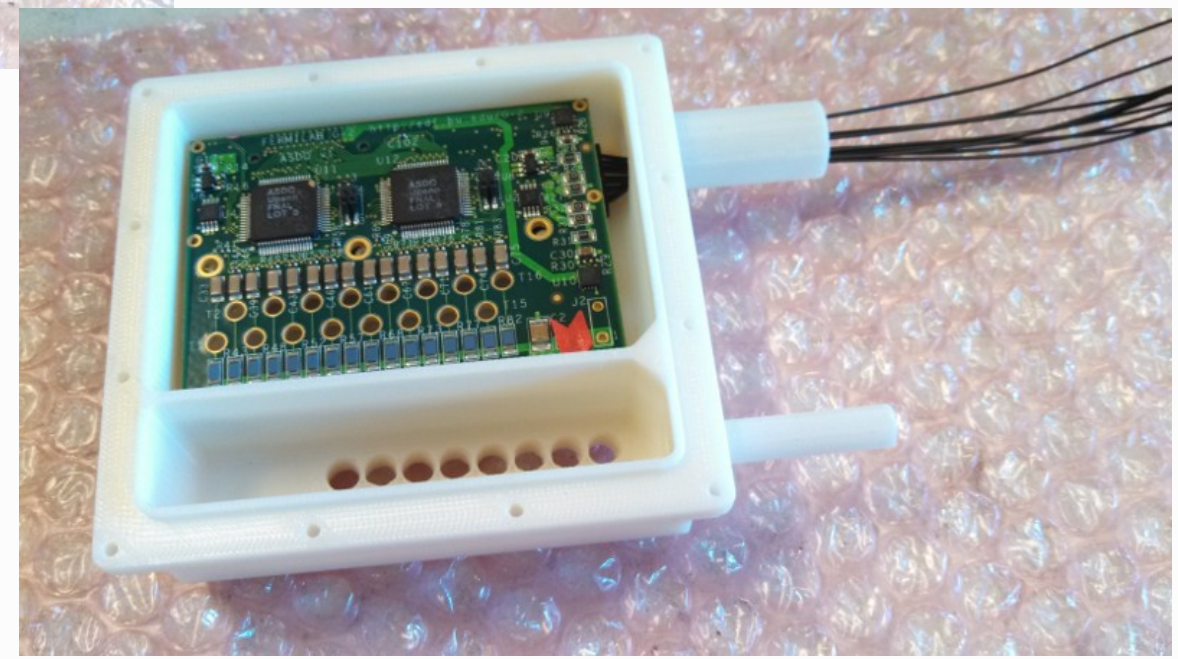
HV in

TDC Board


ASDQ board
Connector (back)
FPGA (TDC)
Test points
Power/
Readout
connector
JTAG
connector

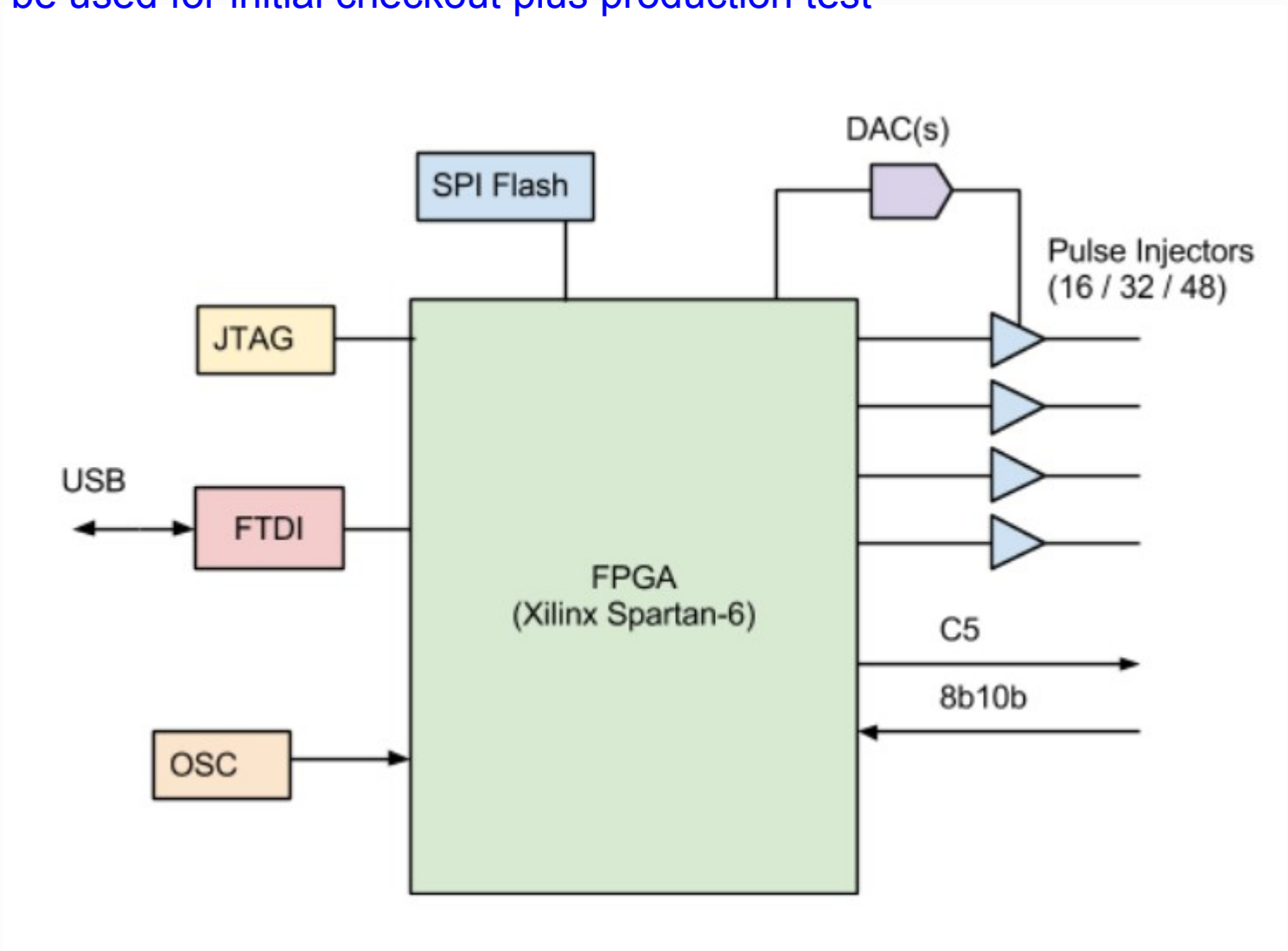
It fits!





“Flight Simulator” test fixture

- Mechanically support ASDQ/TDC board stack
- Provide pulse injection and control/readout
- Can be used for initial checkout plus production test



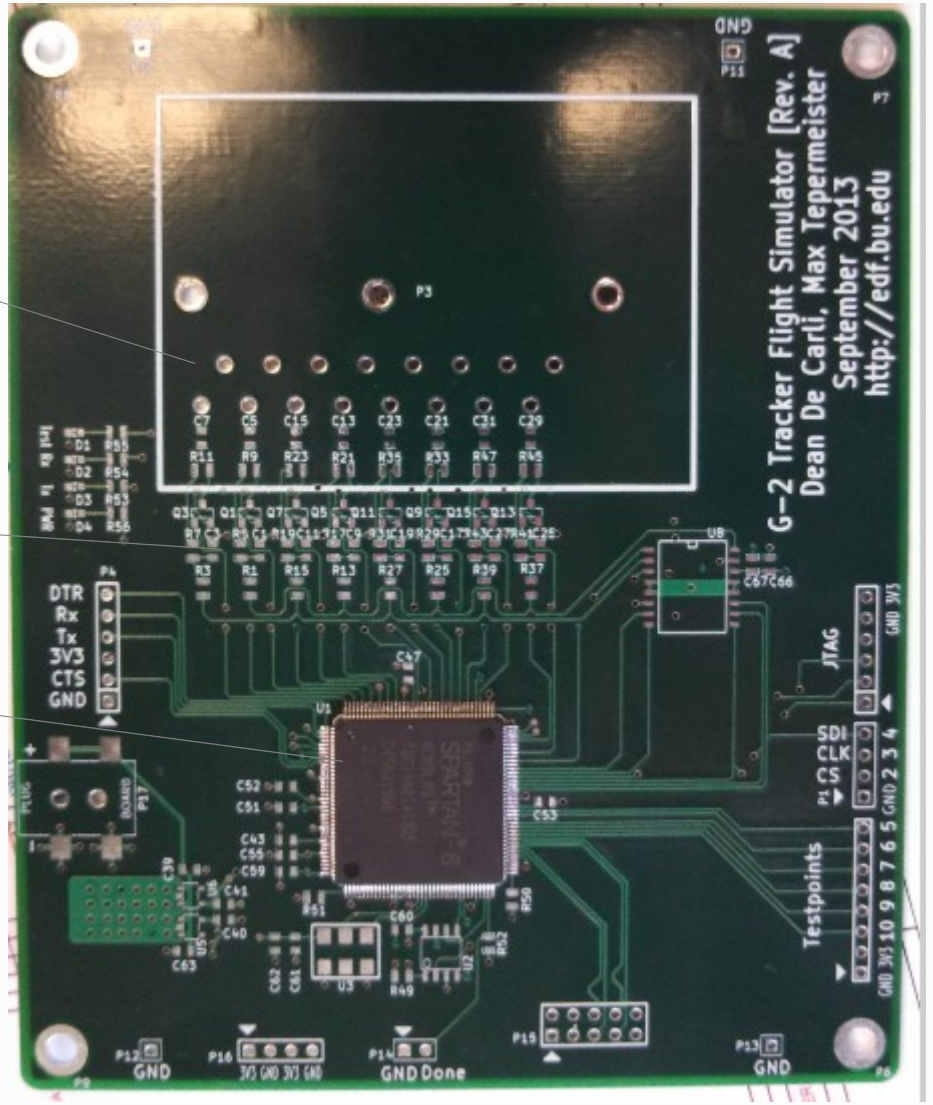
Flight Simulator PCB

- Design and initial layout done (by summer HS intern!)
- USB interface for command / control

ASDQ/TDC
Board stack
Plugs in here

(16) pulse injector
circuits

Spartan-6 FPGA



- Assembly/debug underway
(by EE student)

Commissioning Plan

- TDC Board Alone
  - Install Altera Quartus and make sample design
  - Power up board (carefully) and program/test FPGA
  - Verify power supply voltages
- ASDQ/TDC Board
  - Mount ASDQ board and power up (carefully)
  - Set bias voltages/currents and check all
  - Inject test pulses and look for output
- Get latest TDC design from J.Y.Wu (WH14) and start testing...

This work has just started... Dan G. is taking charge

Tracker DAQ Update

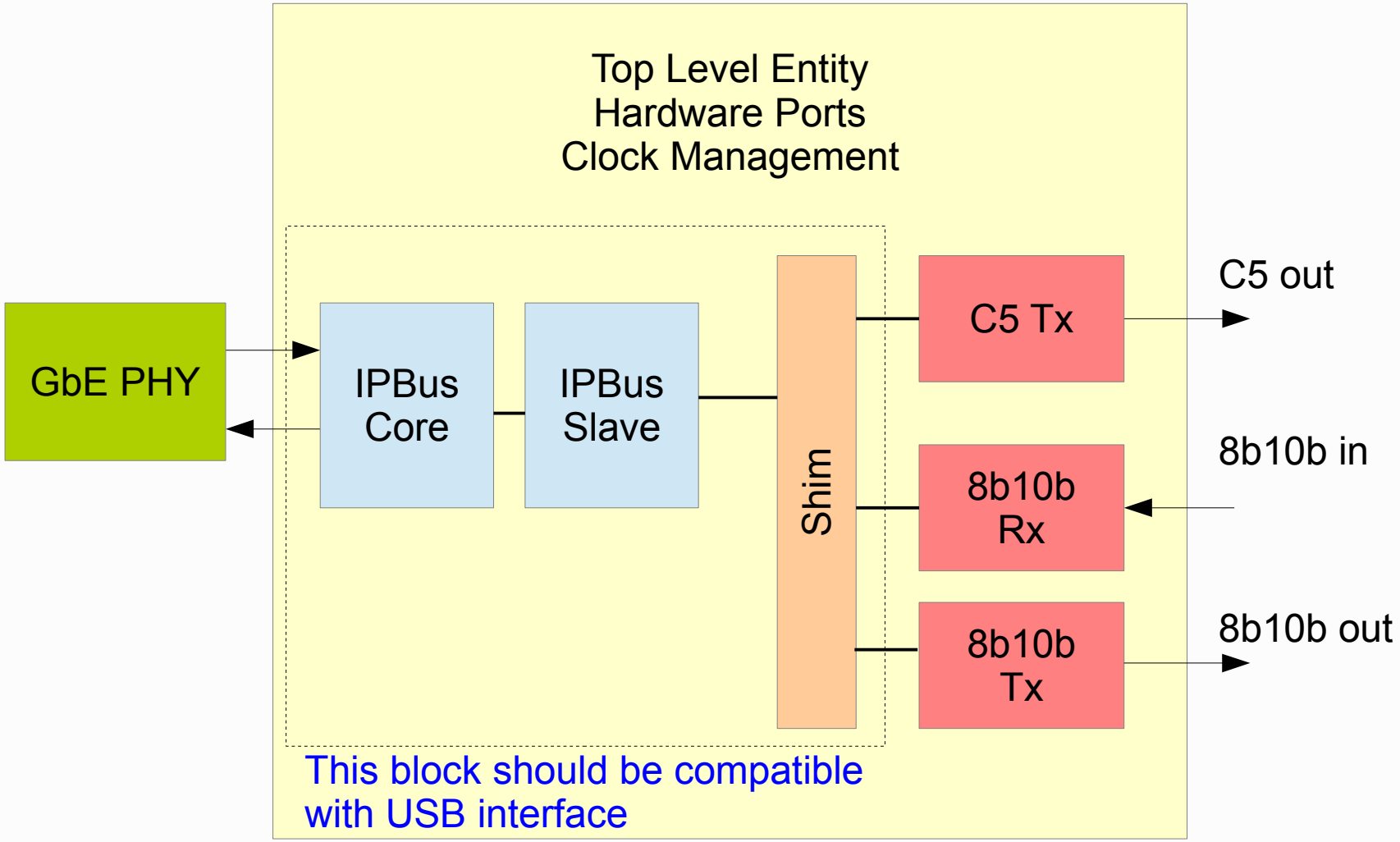
Project Scope

- Firmware and software for Tracker Readout Module
  - Phase zero (*completed*)
    - Digilent Nexys3 based – test TDC design for J.Y. Wu
      - http://edf.bu.edu/svn/edf/G-2/TRM/firmware/trunk/vhdl/
  - Phase I – Underway at Oxford / UCL
    - Digilent Atlys based – one TDC – for test beam
    - Simple uHAL software for testing
    - Some kind of DAQ for test bem
  - Phase II
    - MicroTCA TRM custom hardware
    - More sophisticated firmware with multi-event buffering, interface for multiple TDCs, etc
    - Full G-2 DAQ support

Firmware

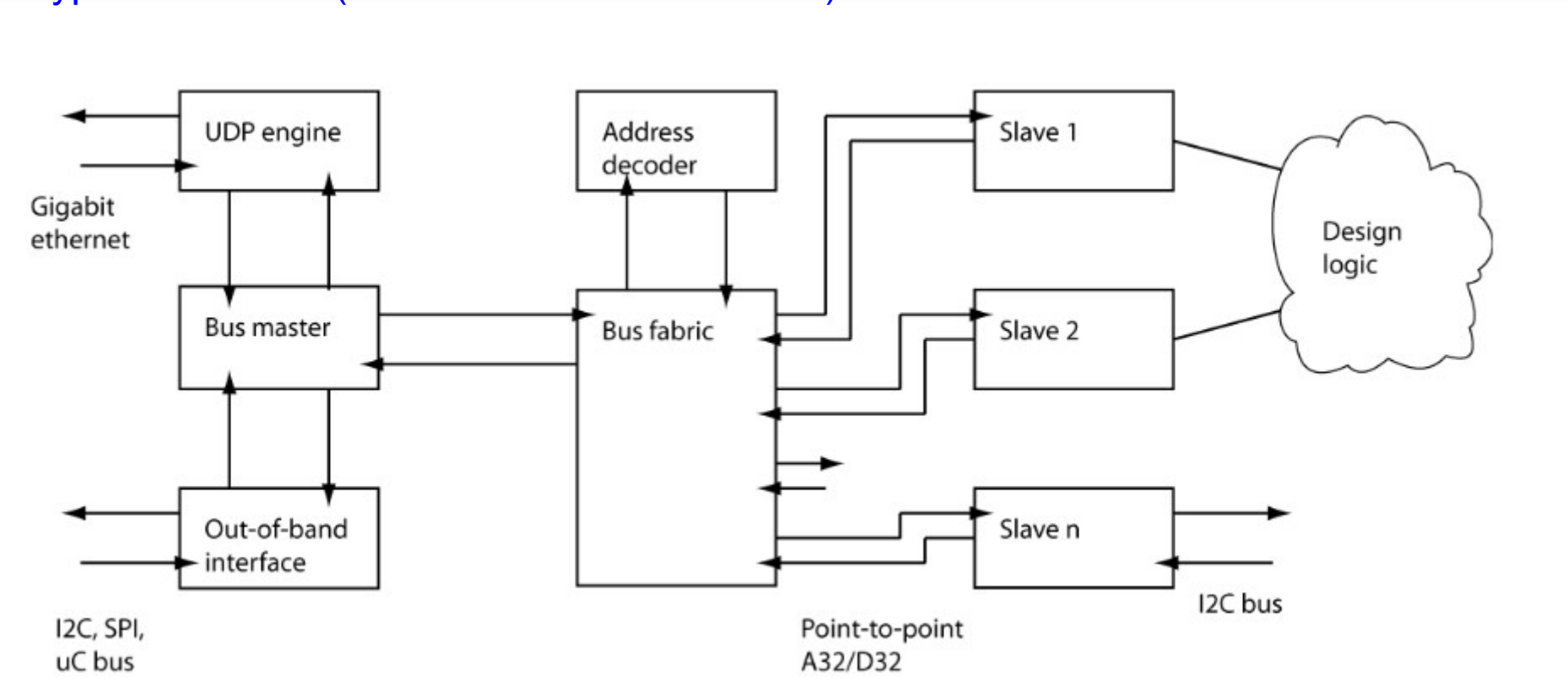
- Status (Phase zero):
  - C5 Sender for commands to TDC: done
  - 8b/10b receiver for TDC data: done
  - USB/Serial interface done
- Phase I and beyond:
  - Initial work started at Oxford and UCL
  - Main short-term goal is to port the Phase zero firmware fro USB to IPBus

Proposed Firmware Structure



IPBus Details

Typical structure (from IPBus documentation)



IPBus Slaves

- Maybe 4?
  - Top-level control/status
  - C5 transmitter
  - 8b10b readout
  - 8b10b test transmitter

Next Steps

- Define IPBus register layout in detail
  - Compatible with DAQ software
  - Consult with Calo guys to maximize common strategies
- Develop initial IPBus firmware for testbeam readout of tracker

Reserve Slides

C5 Transmitter Entity

Inputs all synch'd to 125MHz, 40MHz used only for output
(clock domain crossing handled inside this entity)

```
entity c5_top is

  port (
    clk125 : in  std_logic;                    -- 125MHz clock for computer interface
    clk40  : in  std_logic;                    -- 40MHz clock to run C5 output
    rst_n  : in  std_logic;                    -- active low reset
    din    : in  std_logic_vector(4 downto 0);  -- data in (0:3) plus CTRL
    c5_en  : in  std_logic;                    -- transmit enable
    c5_out : out std_logic);                   -- encoded C5 output

end entity c5_top;
```

8b10b Readout

Data recovery, K.28.5 comma detect, 8b1b0 decoder, 8k byte FIFO
This block requires only 125MHz clock
All control signals 1 clock wide synch'd to clk125 except asynch rst_n

```
entity rec_8b10b_top is

  port (
    clk125     : in  std_logic;          -- system clock
    rst_n      : in  std_logic;          -- active low reset
    serial     : in  std_logic;          -- serial data in
    data_out   : out std_logic_vector(7 downto 0);  -- output data
    fifo_full  : out std_logic;          -- fifo full flag
    fifo_empty : out std_logic;          -- fifo empty flag
    k_char     : out std_logic;          -- K char at FIFO top
    locked     : out std_logic;          -- 8b10b comma aligned
    err        : out std_logic;          -- 8b10b input error
    fifo_wr    : out std_logic;          -- fifo write output for debug
    fifo_clr   : in  std_logic;          -- fifo clear
    test       : out std_logic_vector(4 downto 0);
    fifo_rd    : in  std_logic           -- fifo read strobe
    );

end entity rec_8b10b_top;
```

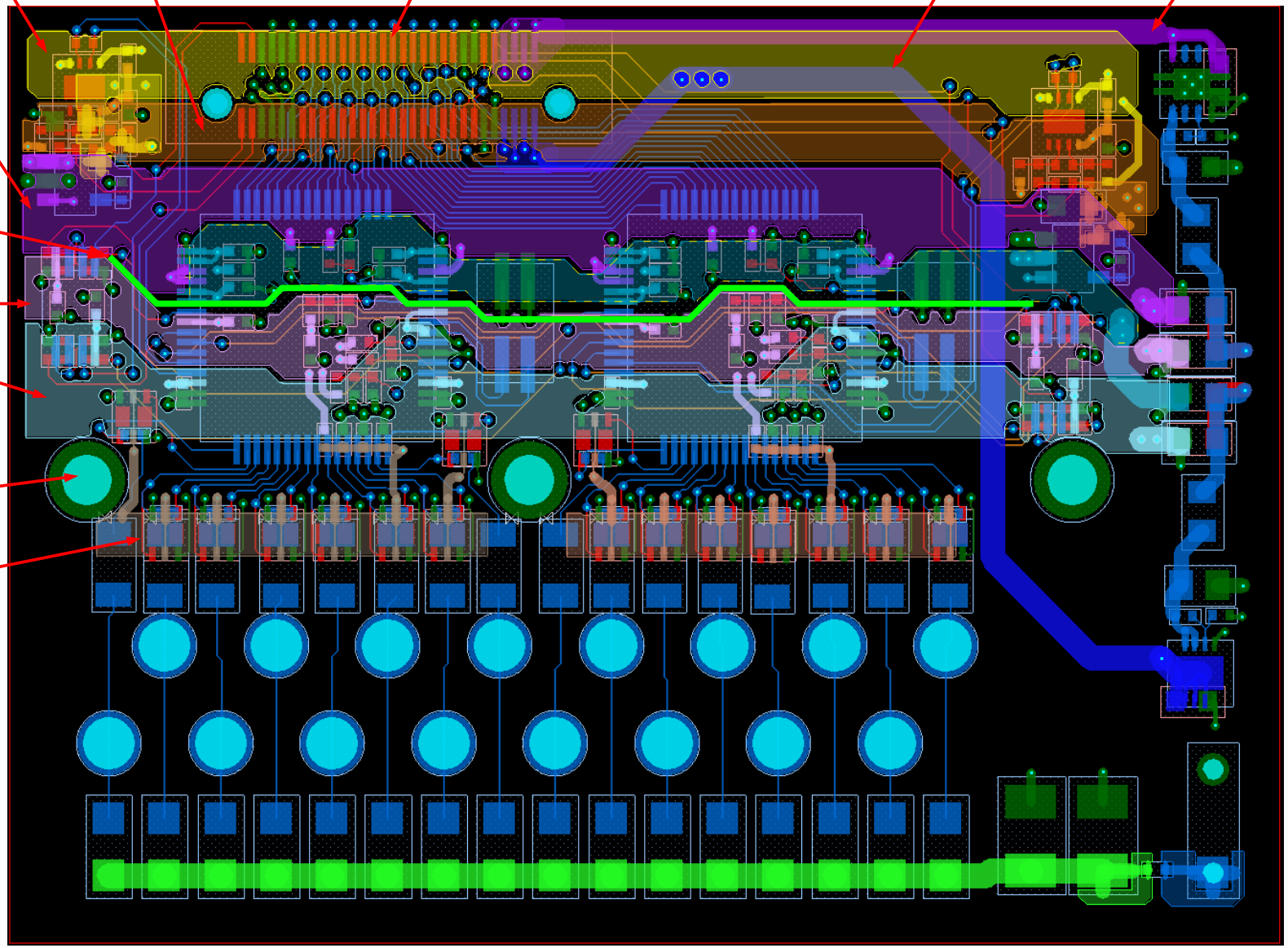
Fake 8b10b Output

Generate simulated TDC data in 8b10b format
Requires 125MHz clock
Output data: header is K.28.5, 0xda, 0xca, 0xfe
Data words are 0xAnnnBnnn
where nnn is hex word number

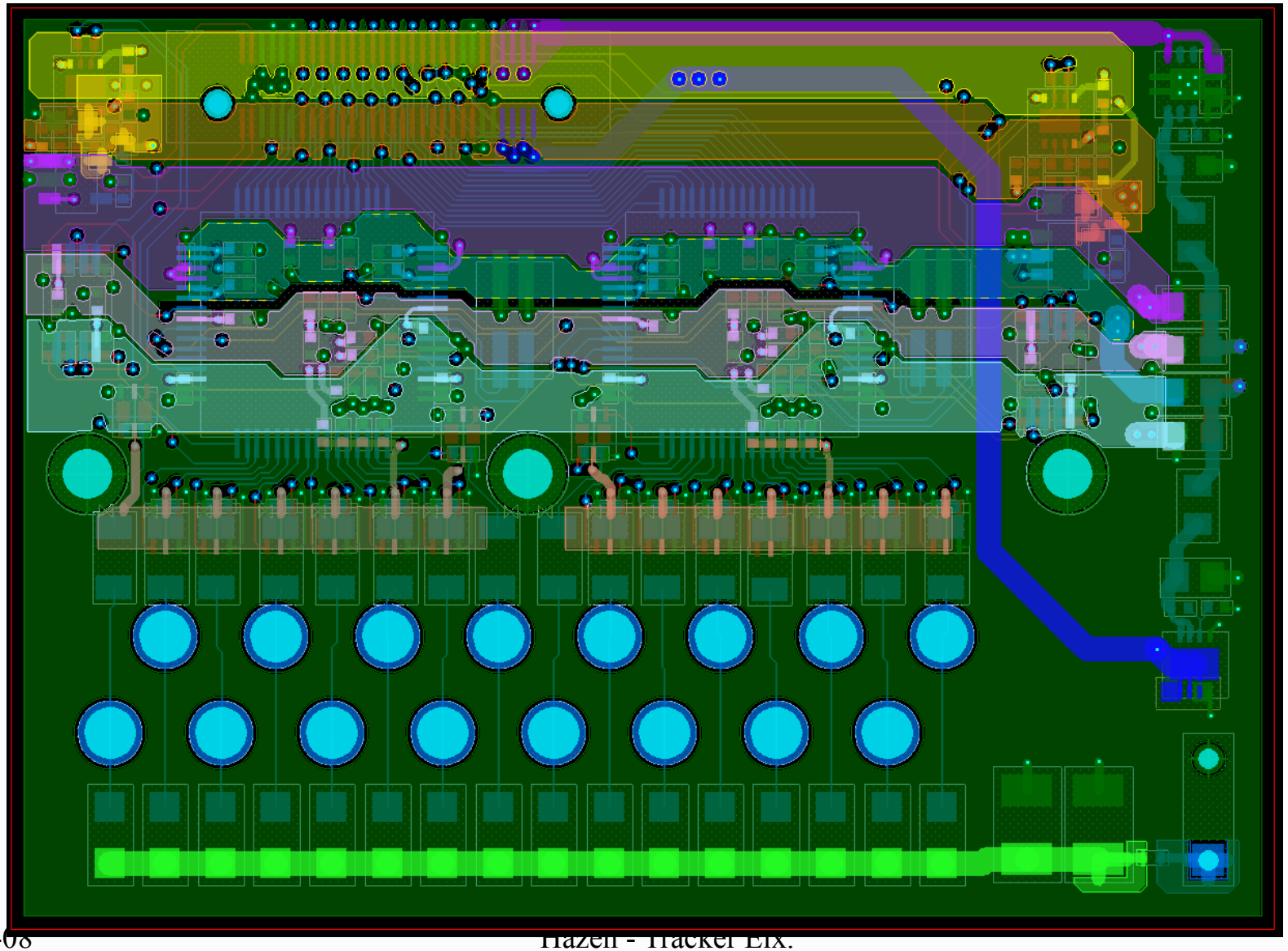
```
entity fake_TDC is

  port (
    clk     : in  std_logic;                     -- 125MHz clock
    rst_n   : in  std_logic;                     -- asynchronous reset
    trig    : in  std_logic;                     -- trigger a fake event
    test    : out std_logic_vector(3 downto 0);  -- debug outputs
    length  : in  std_logic_vector(11 downto 0); -- length in words
    ser_out : out std_logic);                    -- 8b10b serial out

end entity fake_TDC;
```

Note: termination res packs are missing from this view

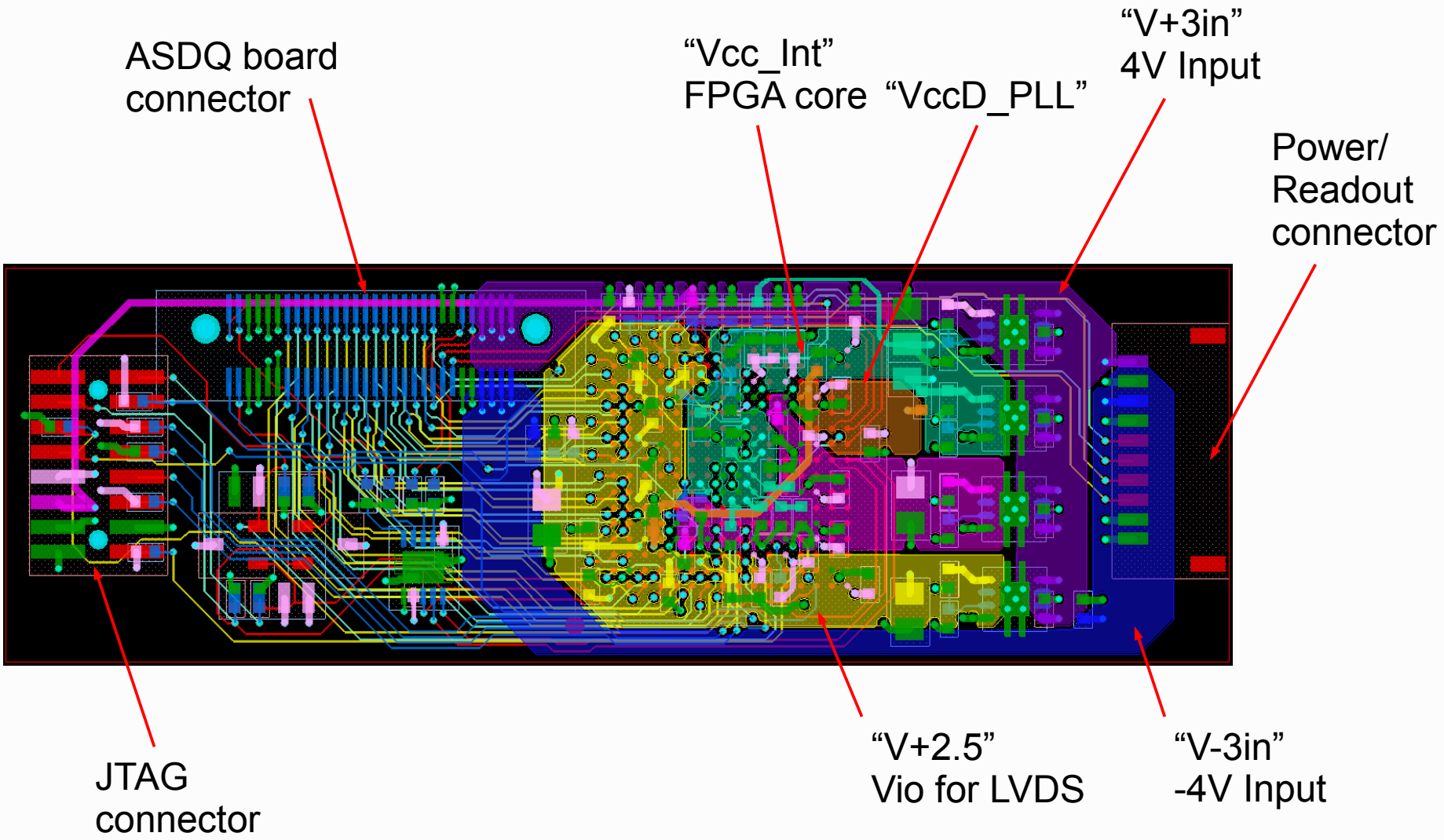
ASDQ Board



All Layers (illustrate A/D split)



TDC Board


ASDQ board
connector
“Vcc_Int”
FPGA core
“VccD_PLL”
“V+3in”
4V Input
Power/
Readout
connector
JTAG
connector
“V+2.5”
Vio for LVDS
“V-3in”
-4V Input